Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-19 (Cancelled)

20. (Previously presented)A method for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter, the method comprising:

receiving an analog differential test signal pair;

converting the analog differential test signal pair into a digital differential test signal pair; and

detecting a differential null condition in the digital differential test signal pair indicating that one of the five fault syndromes has occurred,

wherein detecting includes utilization of a common mode reference voltage.

21. (Previously presented)An apparatus for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter, the apparatus comprising:

means for receiving an analog differential test signal pair;

means for converting the analog differential test signal pair into a digital differential test signal pair; and

means for detecting a differential null condition in the digital differential test signal pair indicating that one of the five fault syndromes has occurred,

wherein detecting includes utilization of a common mode reference voltage.

22. (Previously presented)A receiver for boundary scan testing of differential interconnections between the receiver and a transmitter, the receiver comprising:

a differential input test buffer having null condition detection capability, wherein the differential input test buffer measures a voltage differential between differential inputs and is configured to identify a null condition when the measured voltage differential is less than a threshold voltage; and

an interface mechanism for providing at least partial test coverage for at least one of five fault syndromes associated with the null condition.

23. (Cancelled)

24. (Cancelled)

25. (New) The apparatus as defined in claim 21, wherein the means for detecting comprises means for recovering a test data signal from the transmitter.

26. (New) The apparatus as defined in claim 21 further comprising means for integrating results from the means for detecting, wherein the results are output from the means for integrating.

27. (New) The apparatus as defined in claim 26, wherein the means for integrating preserves incoming signal states in the differential test signal pair during boundary scan testing.

28. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals.

29. (New) The receiver as defined in claim 22, wherein the interface mechanism further comprises a technology mapper for processing one or more output signals from the differential input test buffer into one or more suitable input signals for the interface mechanism.

30. (New) The receiver as defined in claim 22, wherein the interface mechanism further comprises an integrator for processing generated data and fault indicator signals into one or more suitable output signals for the interface mechanism.

31. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals, wherein one of the plurality of detectors is a signal recoverer for recovery of the test data signal from the transmitter.

32. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals, wherein one of the plurality of detectors is an AC short/null detector.

33. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals, wherein one of the plurality of detectors is a DC short detector.

34. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals, wherein one of the plurality of detectors is an AC detector.

35. (New) The receiver as defined in claim 22, wherein the interface mechanism comprises a plurality of detectors for generating data and fault indicator signals, wherein one of the plurality of detectors is a heterogeneous capacitor detector.

36. (New) The receiver as defined in claim 35, wherein the heterogeneous capacitor detector comprises a first flip-flop for sampling a first signal on an even test clock signal, a second flip-flop for sampling a second signal on an odd test clock signal, and a logic gate for combining the outputs of the first and second flip-flops.